LISTING OF THE CLAIMS:

Claims 1-15. (Canceled)

16. (Original) A method for fabricating a semiconductor device, the method comprising:

forming a trench to a depth in a semiconductor substrate;

forming a liner layer formed of a multi-layer of a silicon nitride layer and a silicon oxide layer on the sidewalls and bottom of the trench by atomic layer deposition; and

forming a buried insulating layer filled in the trench without a void.

17. (Original) The method for fabricating a semiconductor device according to claim 16, wherein the liner layer is formed without a vacuum break.

18. (Original) The method for fabricating a semiconductor device according to claim 16, wherein the silicon nitride layer forming the liner layer is formed using silicon source of silane (SiH_4), Si-alkyl, Si-halide, or Si-amide, and a nitrifying agent of ammonia, plasma ammonia, or plasma nitrogen.

19. (Original) The method for fabricating a semiconductor device according to claim 16, wherein the silicon oxide layer forming the liner layer is formed using silicon source of silane (SiH_4), Si-alkoxide, Si-alkyl, Si-halide, or Si-amide, and an oxidizing agent of water (H_2O), hydrogen peroxide, ozone, plasma O_2, N_2O, or plasma N_2O.

20. (Original) The method for fabricating a semiconductor device according to claim 16, wherein an oxide layer is formed by thermal oxidation or atomic layer deposition on the sidewalls and bottom of the trench before a liner layer is formed on the sidewalls and bottom of the trench.

21. (Previously Presented) A method for fabricating a semiconductor device, the method comprising:

forming a trench to a depth in a semiconductor substrate;

forming a liner layer formed of a multi-layer of a silicon nitride layer and a silicon oxide layer on the sidewalls and bottom of the trench by atomic layer deposition; and

forming a buried insulating layer filled in the trench without a void;

forming a plurality of gate stack patterns on the semiconductor substrate in which the trench and the buried insulating layer are formed;

forming a plurality of gate spacers on the sidewalls of the gate stack patterns;

forming a first bubble prevention layer of a multi-layer of a silicon oxide layer and a silicon nitride layer on the gate spacers and the gate stack patterns by atomic layer deposition; and

forming a first filling insulating layer without a void between the gate stack patterns on the first bubble prevention layer.

22. (Previously Presented) The method for fabricating a semiconductor device according to claim 21, wherein the gate spacers are formed by atomic layer deposition of a multi-layer of a silicon oxide layer and a silicon nitride layer.

23. (Original) The method for fabricating a semiconductor device according to claim 21, further comprising the steps of:

forming a plurality of bit line stack patterns on the first filling insulating layer;

forming a plurality of bit line spacers on the sidewalls of the bit line stack patterns;

forming a second bubble prevention layer of a multi-layer of a silicon oxide layer and a silicon nitride layer on the bit line spacers and the bit line stack patterns by atomic layer deposition; and

forming a second filling insulating layer without a void between the bit line stack patterns on the second bubble prevention layer.

24. (Previously Presented) The method for fabricating a semiconductor device according to claim 23, wherein the second bubble prevention layer is formed without a vacuum break.

25. (Previously Presented) The method for fabricating a semiconductor device according to claim 23, wherein the bit line spacers are formed by atomic layer deposition of a multi-layer of a silicon nitride layer and a silicon oxide layer.

26. (Previously Presented) The method for fabricating a semiconductor device according to claim 21, wherein each gate stack pattern is formed by sequentially stacking a gate insulating layer, a first gate conductive layer, a second gate conductive layer, and a gate capping layer.

27. (Original) The method for fabricating a semiconductor device according to claim 26, wherein the gate insulating layer is formed of a silicon oxide layer.

28. (Original) The method for fabricating a semiconductor device according to claim 26, wherein the first gate conductive layer is formed of an impurity-doped polysilicon layer.

29. (Original) The method for fabricating a semiconductor device according to claim 26, wherein the second gate conductive layer is formed of a metal silicide layer.

30. (Original) The method for fabricating a semiconductor device according to claim 26, wherein the gate capping layer is formed of a silicon nitride layer.

31. (Previously Presented) The method for fabricating a semiconductor device according to claim 23, wherein each bit line stack pattern is formed by sequentially stacking a barrier metal layer, a bit line conductive layer, and a bit line capping layer.

32. (Original) A method for fabricating a semiconductor device, the method comprising the steps of:

forming a trench on a semiconductor substrate with a predetermined depth;

forming a liner layer of a multi-layer of a silicon nitride layer and a silicon oxide layer on the sidewalls and bottom of the trench by atomic layer deposition;

forming a buried insulating layer filled in the trench without a void;

forming a plurality of gate stack patterns on the semiconductor substrate on which the trench and the buried insulating layer are formed;

forming a plurality of gate spacers on the sidewalls of the gate stack patterns;

forming a first bubble prevention layer of a multi-layer of a silicon oxide layer and a silicon nitride layer on the gate spacers and the gate stack patterns by atomic layer deposition;

forming a first filling insulating layer without a void between the gate stack patterns on the first bubble prevention layer;

forming a plurality of bit line stack patterns on the first filling insulating layer;

forming a plurality of bit line spacers on the sidewalls of the bit line stack patterns;

forming a second bubble prevention layer of a multi-layer of a silicon oxide layer and a silicon nitride layer on the bit line spacers and the bit line stack patterns by atomic layer deposition; and

forming a second filling insulating layer without a void between the bit line stack patterns on the second bubble prevention layer.

33. (Previously Presented) The method for fabricating a semiconductor device according to claim 32, wherein the liner layer is formed by atomic layer deposition of a multi-layer of a silicon nitride layer and a silicon oxide layer, and the gate spacers and the bit line spacers are formed by atomic layer deposition of a multi-layer of a silicon oxide layer and a silicon nitride layer.

34. (Original) The method for fabricating a semiconductor device according to claim 32, wherein the liner layer, the gate spacers, the first bubble prevention layer, the bit line spacers, or the second bubble prevention layer are formed without a vacuum break.

35. (Original) The method for fabricating a semiconductor device according to claim 32, wherein an oxide layer is formed by thermal oxidation or atomic layer deposition on the sidewalls and bottom of the trench before a liner layer is formed on the sidewalls and bottom of the trench.